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Personal Statement

I am an expert in Microprocessor Logic Design, VLSI Systems, and related intellectual property. Throughout more than twenty years of involvement in the specification, implementation, and debugging of complex computer architecture systems, I've enjoyed the daily challenge of learning, focusing on details, and providing working systems to end customers. In August, 2002, I became a registered US patent agent and intellectual property consultant. I now enjoy aiding clients and their counsel in understanding these technologies, and protecting their intellectual property investments in these areas.

Employment Summary

- 01/2002-present
  - Senior Member Technical Staff, PatentVentures, offices in California and Texas

I am authoring complex patent applications, analyzing existing intellectual property, and expanding the scope of client patent coverage. These contributions are in the areas of complex VLSI system design, leveraging my technical expertise relevant to these systems.

Acting as a technical expert on a licensing project, I analyzed a collection of more than 70 computer microarchitecture patents and related prior art. I identified potentially infringing products based on publicly available information, and produced a collection of associated claim charts. In addition, I assisted the client in drafting further claims targeting other potentially infringing products.

- 10/2001-12/2001
  - Architect, Clearwater Networks (previously XStream Logic), Los Gatos, CA

I was the senior technical contributor in the architecture group. I was responsible for defining, documenting, and championing the architecture of future network processor products.

- 06/2000-09/2001
  - Director, VLSI Development, XStream Logic, Los Gatos, CA

I was responsible for building and leading the VLSI team developing a complex network processor. I owned the overall chip implementation and debug schedule, resource management decisions, and was also the senior technical contributor. The scope of work included front end design, verification, back end design, and debug. I built the team from ten to 35 members, and increased the skill set from front end logic design and EDA to include circuit, micro-architecture, and verification. In addition, I lead a "virtual ops" group until the operations team came on board.

- 06/1999-05/2000
  - Senior Manager, Architecture, ATI Research Silicon Valley, Santa Clara, CA

Previous positions (at ATI):
- Manager, ATI Research Silicon Valley, Santa Clara, CA

I was responsible for the top-level CPU architectural definition and partitioning, working directly with a technical writer to specify the architecture unambiguously. This requires a micro-code programmer's model negotiated between the micro-code and hardware micro-architecture implementers and logic designers. I lead the micro-code development and performance analysis teams. I also directly managed the place and route group.

I was responsible for leading a cross-functional team to design in complete X86 compatibility. This requires investigations into ambiguous or complex cases, specifying the architecture of the solution (hardware and/or software), and coordinating the complex hardware/software solutions.

I worked with contributors across the CPU to encourage and facilitate filing patent applications covering the inventions at architectural and implementation levels.

I led a small team designing the pipeline control section of a super-scalar in-order x86 compatible processor. The team was responsible for unit definition and micro-architecture, block partitioning, RTL coding, synthesis, custom macro-specification, timing analysis and improvement, cell placement, and cell routing. The team was charged with meeting area, timing, and bug count goals. I coordinated the activities of the group and negotiated interfaces with the other three units of the processor: memory, instruction fetch/conversion, and datapaths, in addition to providing specific technical guidance and solving problems.

- 05/1996-5/1999
  - Member Technical Staff, Architect, Chromatic Research, Sunnyvale, CA (merged with ATI Technology Nov 1998)

I drove closure of the final details of the programmer's model of a complex instruction set architecture device with multiple processors. Each processor is super-scalar (in order), dual instruction set capable (industry standard X86 plus proprietary native), with hardware optimizations to support binary translation and media operations (MPEG decoding and encoding, decryption, and 3D lighting and geometry calculations).

I was a key contributor to the team refining the product definition, system and CPU level partitioning, CPU ISA, and internal CPU micro-architecture. I personally connected logic and circuit designers with media programmers via negotiation and analysis to enable a high performance well thought out and cost effective total solution.

I examined external intellectual property to identify exposures and workarounds. I contributed directly to the creation of internal intellectual property: multiple ISA execution, hardware optimization for binary translation, video decoding ISA optimization, X86 compatible ISA implementation techniques, standard PC sub-system virtualization mechanisms, and compatible segmentation and paging methods.

- 10/1987-05/1996
  - Senior Manager, AMD (formerly Nexgen), Milpitas, CA

Previous positions (at Nexgen):
- Director Processor Development
- Project manger Architecture Development
- Senior Member Technical Staff
- Member Technical Staff

I investigated possible micro-architectures for the eighth generation x86 ISA implementation, including: overall CPU performance (using an in-house performance simulation tool), expected cycle time (based on logic design of critical paths), and required process technology.

I was a key contributor toward the first Nexgen product (Nx586) – a super-scalar, out of order, fifth generation implementation of the x86 ISA. This product briefly shipped to customers.

My individual contributions included: pipeline control logic design, branch prediction and multiple stream instruction fetch micro-architecture and logic design, lab debug, timing bug identification and resolution, performance analysis and improvement, and overall design correctness.

Management responsibilities included: architectural verification, lab debug, and eventually the entire implementation of the CPU in groups from 4 to 20 people.

- 6/1982-10/1987
  - VLSI Systems Engineer, VLSI Technology, San Jose, CA

I led a small team as an active manager in the design, implementation, and prototype evaluation of a programmable digital signal processor. The project began with the definition of the instruction set architecture, and culminated in a working modem demonstration constructed from the first silicon.

I specified and designed the memory interface for a multi-mode display interface chip (first silicon was used for product demonstration), reverse engineered a small CMOS standard part chip, and supported a telecommunications chip set customer design project.

- 6/1981-6/1982
  - Research Assistant, UC Berkeley, Berkeley, CA

I assisted in the NMOS logic specification, logic verification, functional simulation, circuit design, and layout verification of an implementation of a Reduced Instruction Set Computer (RISC-I).

Education

6/1982	MS, EECS	UC Berkeley, Berkeley, CA	GPA: 4.0/4.0
6/1980	BS, EECS	UC Berkeley, Berkeley, CA	GPA: 3.9/4.0

Patents

The following page provides a complete listing of patents for which I am a co-inventor (as of March, 2003). These patents relate to a variety of subjects, including: multiple ISA execution, hardware optimization for binary translation, video decoding ISA optimization, compatible ISA implementation techniques, speculative instruction execution, branch prediction, compatible segmentation and paging, standard PC sub-system virtualization, address generation, and logarithmic calculation.

Activities

I have been inducted into: Phi Beta Kapa, Tau Betta Pi , and Eta Kappa Nu
I am a member of IEEE (since 1978)
I am a member of ACM (since 1983)

References

Brad Howe, VP of Engineering at Clearwater/XStreamLogic (my direct supervisor at Clearwater/XStream)
Jeff Thomas, VP of Engineering at ATI.Chromatic (my direct supervisor Chromatic/ATI)
Dave Epstein, VP of Engineering at NexGen (my direct supervisor at NexGen)

Issued Patents (co-inventor)	
Number	**Title**
6,499,123	Method and apparatus for debugging an integrated circuit
6,449,671	Method and apparatus for busing data elements
6,430,646	Method and apparatus for interfacing a processor with a bus
6,425,075	Branch prediction device with two levels of branch prediction cache
6,418,524	Method and apparatus for dependent segmentation and paging processing
6,397,379	Recording in a program execution profile references to a memory-mapped active device
6,360,318	Configurable branch prediction for a processor performing speculative execution
6,324,635	Method and apparatus for address paging emulation
6,321,314	Method and apparatus for restricting memory access
6,282,639	Configurable branch prediction for a processor performing speculative execution
6,212,629	Method and apparatus for executing string instructions
6,195,745	Pipeline throughput via parallel out-of-order execution of adds and moves in a supplemental integer execution unit
6,108,777	Configurable branch prediction for a processor performing speculative execution
6,067,616	Branch prediction device with two levels of branch prediction cache
5,881,265	Computer processor with distributed pipeline control that allows functional units to complete operations out of order while maintaining precise interrupts
5,815,699	Configurable branch prediction for a processor performing speculative execution
5,802,339	Pipeline throughput via parallel out-of-order execution of adds and moves in a supplemental integer execution unit
5,781,753	Semi-autonomous RISC pipelines for overlapped execution of RISC-like instructions within the multiple superscalar execution units of a processor having distributed pipeline control for speculative and out-of-order execution of complex instructions
5,768,575	Semi-Autonomous RISC pipelines for overlapped execution of RISC-like instructions within the multiple superscalar execution units of a processor having distributed pipeline control for sepculative and out-of-order execution of complex instructions
5,748,932	Cache memory system for dynamically altering single cache memory line as either branch target entry or prefetch instruction queue based upon instruction sequence
5,682,492	Computer processor with distributed pipeline control that allows functional units to complete operations out of order while maintaining precise interrupts
5,675,758	Processor having primary integer execution unit and supplemental integer execution unit for performing out-of-order add and move operations
5,649,137	Method and apparatus for store-into-instruction-stream detection and maintaining branch prediction cache consistency
5,623,614	Branch prediction cache with multiple entries for returns having multiple callers
5,590,351	Superscalar execution unit for sequential instruction pointer updates and segment limit checks
5,515,518	Two-level branch prediction cache
5,511,175	Method an apparatus for store-into-instruction-stream detection and maintaining branch prediction cache consistency
5,454,117	Configurable branch prediction for a processor performing speculative execution
5,442,757	Computer processor with distributed pipeline control that allows functional units to complete operations out of order while maintaining precise interrupts
5,327,547	Two-level branch prediction cache
5,230,068	Cache memory system for dynamically altering single cache memory line as either branch target entry or pre-fetch instruction queue based upon instruction sequence
5,226,130	Method and apparatus for store-into-instruction-stream detection and maintaining branch prediction cache consistency
5,226,126	Processor having plurality of functional units for orderly retiring outstanding operations based upon its associated tags
5,163,140	Two-level branch prediction cache
5,109,524	Digital processor with a four part data register for storing data before and after data conversion and data calculations