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EMPLOYMENT SUMMARY

I am an independent consultant in integrated circuit microarchitecture, microprocessors, computing-platforms, and related intellectual property. I am a co-inventor on five branch-prediction patents. I am also a registered U.S. Patent Agent. I have written specifications or contributed strategic claims in many issued patents and pending patent applications in the computer arts. Since 1998, my consulting practice has specialized in developing patent applications and providing related advice for well-funded computer, communications, and networking start-ups, who appreciate the extra value of my simultaneous expertise in both computer engineering and patent practice, and who consider building a quality patent portfolio to be of major importance. I am a member of the IEEE. I am married and have four children.

I received a BSEE in 1980 from Texas A&M and subsequently worked as an IC designer at Texas Instruments and Hewlett-Packard. In 1984, I received an MSEE from UC Berkeley, where I studied microprocessor logic design and wrote a thesis under Nick Tredennick. I worked on processor projects at the IBM T.J. Watson Research Center (on the Micro/370) during 1984-1987 and at NexGen (on the Nx586, as employee number 6) during 1987-1989. I did design and intellectual property consulting during 1989-1992 for Tredennick, Incorporated. I became a Patent Agent in December 1992. I managed NexGen's intellectual property activities during 1993-1995. I was a consultant to AMD’s CTO during 1996-1998. I co-authored (with Dr. Bruce Shriver) a graduate-level text: “The Anatomy of a High-Performance Microprocessor: A Systems Perspective,” published by the IEEE Computer Society Press, in 1998.

EMPLOYMENT HISTORY

(January 1993 to present)
Consultant in Computers & Related Intellectual Property
(Operating as a Sole-Proprietor first in San Jose, CA; then in Palo Alto, CA; and currently in Georgetown, TX)

In March 2001, I relocated to Georgetown, TX, near Austin. I continue to service clients in CA.

Since 1998, I have worked as a consultant and patent agent in computer matters and related intellectual property for clients that have included: Raycer Graphics (a Palo Alto, CA graphics accelerator start-up acquired by Apple), HotRail (formerly known as Poseidon Technologies, a San Jose, CA multiprocessor-chipset and network-switching-chipset start-up acquired by Connexant), Socket Communications (a Fremont, CA PDA-expansion-module developer), Busless SARL (a French multiprocessor and memory component company), Pacific Broadband Communications (a San Jose, CA and French Cable-Modem-systems start-up acquired by Juniper Networks), and Fotiva (formerly known as PhotoTablet, a Santa Rosa, CA digital photography start-up acquired by Adobe).

In 1998, I co-authored (with Dr. Bruce Shriver) a graduate-level text: “The Anatomy of a High- Performance Microprocessor: A Systems Perspective”, published by the IEEE Computer Society Press. This was a Computer Society Press best-seller in 1999. The book was done as an hourly consulting project for AMD. I wrote chapters 4 through 6, and portions of chapter 1 (particularly the section on PC platforms).

From mid-January 1996 through mid-1998, I was on the staff of the Advanced Architecture Lab of Advanced Micro Devices (AMD), focused on future computing platforms. I reported directly to Atiq Raza, the Chief Technical Officer (CTO) of AMD.

In 1996, I relocated to Palo Alto, CA.

During February through early August 1996, I was a pre-trial defense expert witness for S3’s counsel in litigation brought by Brooktree over U.S. Patent 5,406,306.

During the period of June of 1994 through mid-January 1996, I coordinated the Intellectual Property activities of NexGen, Inc. My responsibilities included portfolio management, patent prosecution, management of patent related work done by multiple outside law-firms, hosting of IP due diligence audits, review of competitive patents, technical analysis of patents for opinion letters by outside counsel, acting as an interface to the engineering staff for patent matters, and various special projects. I hosted the IP due diligence audit that culminated in NexGen's acquisition by AMD in January 1996. I reported directly to Atiq Raza, the President & CEO of NexGen. I acted as agent for the following issued patents: 5,623,614; 5,590,351; 5,517,440; 5,454,117; 5,418,736 and 5,394,351. I had a significant role in drafting claims or responses to Office Actions in the following issued patents: 5,583,806; 5,515,518; 5,513,330; 5,511,175; 5,442,757; 5,414,820 and 5,369,748.

During all of 1993-1995, I was an expert in a pre-litigation matter involving x86-related microprocessor patents. My responsibilities included: explaining computer patents; performing computer tutorials; drafting reports, position papers, and declarations; invalidity analysis; claim reading; prior art searches; competitive product analysis; and drafting of strategic patent claims and applications.

I started my independent consultancy in San Jose, CA in January 1993.

(August 1989 to December 1992) Member Technical Staff, <u>Tredennick, Inc.</u>, San Jose, California. (*Tredennick, Inc. is a small logic design and consulting firm owned and operated by Nick Tredennick.)*

I became a registered Patent Agent in December 1992.

I was an expert to OPTi's counsel in the Chips and Technologies vs. OPTi memory-controller patent and trade secret case. I also was an expert to ULSI's counsel in the Intel vs. ULSI floating-point coprocessor patent infringement suit. I wrote an affidavit and gave deposition testimony supporting "USLI's Opposition to Intel's Motion for Preliminary Injunctive Relief."

I performed architectural evaluations and wrote position papers as part of Hitachi's technical preparation for the Motorola vs. Hitachi Patent License Agreement (PLA) Litigation.

I was Project Leader for a "clean-room" gate-level definition of a high-performance microcontroller, compatible to the 8051 architecture. I supervised seven engineers. I designed the CPU-partition of the microcontroller. This included the logic design of its sequencer and datapath, and the writing of its microcode. I also designed the microcontroller's four Timers and UART.

I performed many patent prior-art searches and patent-related product analyses related to both litigations and license agreements.

(March 1987 to August 1989) Senior Member Technical Staff,
Nx586 Processor, NexGen, Inc., Milpitas, California. (*NexGen developed high-performance x86 microprocessors. NexGen has since been acquired by AMD.)*

I joined NexGen as its 6th employee. I managed a small team working on the Floating-Point Execution Unit during its initial definition and contributed to the development of a microcode design specification for it. I also designed a multi-cycle sequencer for the Integer Execution Unit and co-designed the IFetch Unit. While working on the IFetch Unit, I wrote an architectural specification detailing numeric coprocessor compatibility issues and co-invented the integrated single-structure branch prediction cache used in the Nx586.

(June 1984 to March 1987) Senior Associate Engineer,
Specifications and Structures Project (Micro/370), Microsystems Department,
Large Systems and VLSI Group, Computer Sciences Department,
Thomas J. Watson Research Center, Research Division,
International Business Machines Corporation, Yorktown Heights, New York.

I wrote experimental floating-point and decimal microcode for the Micro/370, a microprocessor that implements the System/370 Architecture. I also did PLA generation, ground-rule checking, transistor extraction, and switch level simulation, all for the Micro/370 project. I also designed and coded in-part an experimental PC-based microcode editor to support Nick Tredennick's Hardware Flowchart Method of microprocessor design.

**(August 1981 to May 1984) Development Engineer (MTS),
Data Terminals Division (which became the Generals Systems Division,
and then the Personal Computer Division),
Computer Group, Hewlett-Packard Company, Sunnyvale, California.**

In 1984, I received an MSEE from UC Berkeley, while working for Hewlett-Packard. I studied advanced analog and digital MOS integrated circuit design. I also studied microprocessor logic design under Nick Tredennick, the microarchitect of the Motorola 68000. Dr. Tredennick, who was on a teaching sabbatical from IBM Research, supervised my thesis (along with Dr. Dave Hodges of Berkeley). The thesis project was directed toward the development of a processor to implement the decimal instructions of the System/370 Architecture. The project required me to specify microcode and microcode-field control-decoders to reconfigure the Micro/370 microprocessor as a decimal coprocessor.

My work at Hewlett-Packard was on early-stage chip definition, cost-reduction studies, and experimental circuitry related to analog and digital ICs and hybrids for Cathode-Ray-Tube (CRT) monitors used in raster-mode computer displays. These activities dealt with attempts to integrate portions of various display subsystems, including high and low-voltage power supplies, sweep generators, and dot-clock-rate video. I was also involved in compilation of related specifications for CRT vendors.

**(May 1980 to August 1981) IC Design Engineer, Telecom Section,
Consumer Systems Branch, Circuits Design and Development Department,
Semiconductor Group, Texas Instruments, Dallas, Texas.**

I worked on the early-stage circuit-design of a CMOS Op-Amp, using SPICE. I graduated from the T.I. Front End *(IC fab)* Engineering Training Program. I supervised two engineering technicians. I evaluated and characterized switched-capacitor filter circuits for the TCM2912 CODEC filter project.

EMPLOYMENT DURING COLLEGE

(1977 through 1980) Engineering Student-Trainee (Co-Op), Microelectronics Section, Sensor Systems Branch, Experiments Systems Division, Engineering and Development Directorate, NASA-Johnson Space Center, Houston, Texas.

I worked at the NASA Johnson Space Center during 3 separate semester-long assignments. During the first assignment, I learned many processes and techniques for Thick-Film Hybrid-Microcircuit fabrication and evaluation. During the second assignment, I worked in an IC fab, learning oxidation processes and techniques for MOS device fabrication and evaluation. During the last assignment, I developed program flow-charts and wrote experimental routines (in RCA CDP1802 assembly code) for the Space Shuttle Small Camera Intervalometer (a programmable controller for specialized time-lapse photography).

OTHER ACCOMPLISHMENTS, SKILLS AND INTERESTS

- I passed the Fundamentals of Engineering *(EIT)* Examination in Texas on November 3, 1979. I pass the Principles and Practice *(national)* Examination *(Electrical Branch)* in Texas on November 1, 1980.
- I have been inducted into: Eta Kappa Nu, Tau Beta Pi, Phi Kappa Phi, Phi Eta Sigma.
- I am a member of the IEEE.
- I am a member of the Silicon Valley Intellectual Property Law Association (SVIPLA).
- I am a lay member of the Santa Clara County Bar Association's High Tech Law Section.
- I am a lay member of the State Bar of California's Intellectual Property Section.
- I have attended many Patent Resource Group Seminars, including: Advanced Patent Application and Amendment Writing, Patent Litigation, and Designing Around Valid U.S. Patents.